REMARKS

The Office Action dated November 23, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-48 are pending with claims 30-48 withdrawn from consideration. By this Amendment, claims 18, 24 and 25 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-48 are pending in the present application and claims 18-25, 28 and 29 are respectfully submitted for consideration.

Allowed Claims and Allowable Subject Matter

As a preliminary matter, Applicant appreciates the allowance of claims 1-17, 26 and 27 and the indication of allowable subject matter in claims 19-21 of the present application.

Claims 18, 22-25, 28 and 29 Rejected Under 35 U.S.C. §102(b)

Claims 18, 22-25, 28 and 29 were rejected under 35 U.S.C. §102(b) as being anticipated by Akiyama, Hideki (JP-05053857 A). Applicant respectfully traverses the rejection and submits that each of claims 18, 22-25, 28 and 29 recites subject matter that is neither disclosed nor suggested in this cited prior art.

Claim 18 recites an electronic device comprising, among other features, a second semiconductor device having an input circuit connected to the bus line for holding a first bus line signal on the bus line in response to a supply of the first logical output signal from the first semiconductor device; and a second output circuit connected

to the input circuit for supplying the bus line with the held first bus line signal following to a supply of the second logical output signal from the first semiconductor device, wherein the comparison circuit receives a second bus line signal from the second output circuit and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Claim 24 recites a first semiconductor device comprising, among other features, a comparison circuit connected to the bus line, that receives a second bus line signal on the bus line in response to an output of the second logical output signal from the second semiconductor device and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Claim 25 recites a first semiconductor device comprising, among other features, an output circuit connected to one of the plurality of bus lines that supplies the bus line with a first logical output signal and, thereafter, supplies a second logical output signal being an inverted signal of the first logical output signal, wherein the second semiconductor device receives a first bus line signal on the bus line in response to a supply of the first logical output signal from the output circuit, and wherein the second semiconductor device holds a first bus line signal on the bus line in response to a supply of the first logical output signal from the first semiconductor device and supplies the bus line with the held first bus line signal following a supply of the second logical output signal from the first semiconductor device; and a comparison circuit connected to the bus line, that receives a second bus line signal from the second semiconductor

device and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

Applicant submits that Akiyama fails to disclose or suggest each and every element recited in claims 18, 24 and 25 of the present application. In particular, it is submitted that the circuit for testing connection between LSI is neither comparable nor analogous to the test method and test circuit for electronic device of the present invention.

In fact, Applicant submits that Akiyama fails to disclose at least, 1) an input circuit for holding a first bus line signal on a bus line in response to a supply of a first logical output signal from the first semiconductor device, 2) a second output circuit for supplying the bus line with the held first bus line signal following a supply of a second logical output signal from the first semiconductor device, and 3) a comparison circuit for receiving a second bus line signal from the second output circuit and comparing the first logical output signal and the second bus line signal to generate a judgment signal with respect to claim 18.

Furthermore, Applicant submits that Akiyama fails to disclose at least a comparison circuit for receiving a second bus line signal from the second semiconductor device, which holds a first bus line signal on the bus line in response to a supply of the first logical output signal from the first semiconductor device and supplies the bus line with the held first bus line signal following a supply of the second logical output signal from the first

semiconductor device, and comparing a first logical output signal and the second bus line signal to generate a judgment signal with respect to claim 25.

Moreover, it is submitted that Akiyama does not disclose at least a comparison circuit for receiving a second bus line signal on the bus line in response to an output of a second logical output signal, which is an inverted signal of a first bus line signal, from the second semiconductor device and compares the first logical output signal and the second bus line signal to generate a judgment signal with respect to claim 24.

In view of the above, Applicant submits that Akiyama fails to disclose each and every element recited in claims 18, 24 and 25 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Akiyama fails to disclose or suggest each and every feature of claims 18, 25 and 26. Accordingly, Applicant respectfully submits that claims 18, 25 and 26 are not anticipated by nor rendered obvious by the disclosure of Akiyama. Therefore, Applicant respectfully submits that claims 18, 24 and 25 are allowable.

Claims 19-21 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 19-23, 28 and 29 depend from claim 18. Applicant respectfully submits that claims 19-23, 28 and 29 are allowable due to their dependency from allowable claim 18.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

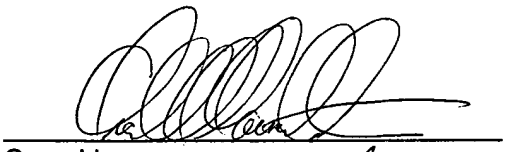
Conclusion

In view of the above, Applicant respectfully submits that each of claims 18-25, 28 and 29 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 18-25, 28 and 29 be found allowable and that this application be passed to issue with allowed claims 1-17 and 26-27.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-09034.**

Respectfully submitted,



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Enclosures: RCE Transmittal
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